WE CLAIM:

1. An integrated circuit capacitor comprising:

a first metal layer with a top surface;

an etch-stop/barrier layer above said first metal layer;

a conductive layer above said etch-stop/barrier layer;

a dielectric layer above said etch-stop/barrier layer and said conductive layer; and

a second metal layer above said dielectric layer.

2. The integrated circuit capacitor of claim 1 wherein said first and second metal layers are copper.

3. The integrated circuit capacitor of claim 2 wherein said conductive layer is a material selected from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys.

4. The integrated circuit capacitor of claim 3 wherein said etch-stop/barrier layer is silicon nitride.

5. An integrated circuit capacitor comprising:

a copper layer with a top surface;

a conductive layer with bottom surface; and

an etch-stop/barrier dielectric layer wherein a portion of said etch-stop/barrier dielectric layer is adjacent to said top surface of said copper layer and to said bottom surface of said conductive layer.

6. The integrated circuit capacitor of claim 5 wherein said conductive layer is a material selected from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys.

7. The integrated circuit capacitor of claim 6 wherein said etch-stop/barrier dielectric layer is silicon nitride.

8. The integrated circuit capacitor of claim 6 wherein said etch-stop/barrier dielectric layer comprises a plurality of dielectric films with varying dielectric constants.

9. A method of forming an integrated circuit capacitor comprising:

providing a silicon substrate with a first dielectric film containing at least one copper layer;

forming a second dielectric layer over said first dielectric layer and said copper layer;

forming a first conductive layer over said first dielectric layer; and

removing a region of said first conductive layer such that a portion of said second dielectric layer remains between said first conductive layer and said copper layer.

10. The method of claim 9 further comprising:

forming copper contacts to said first conductive layer; and

forming a second copper layer that electrically contacts said copper contacts.

11. The method of claim 9 wherein said first conductive layer is formed from a material selected from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys.

12. The method of claim 9 wherein said second dielectric layer is formed using at least two different dielectric films.

13. The method of claim 9 wherein said second dielectric layer is an etch-stop/barrier layer.

14. The method of claim 9 wherein said second dielectric layer is silicon nitride.

15. A stacked integrated circuit capacitor comprising:

a plurality of copper layers;

a plurality of conductive layers;

a plurality of dielectric etch-stop/barrier layers positioned between each pair of said plurality of copper layers and said plurality of conductive layers; and

interconnecting said plurality of copper layers and said plurality of conductive layers to form a stacked capacitor structure.

16. The stacked integrated circuit capacitor of claim 15 wherein said plurality of conductive layers are materials selected from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys.

17. The stacked integrated circuit capacitor of claim 15 wherein said plurality of dielectric etch-stop/barrier layers is silicon nitride.